| REVISIONS | | | |
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| LTR | DESCRIPTION | DATE | APPROVED |
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**MIL-S-19500/440 has been cancelled.**
**This drawing may be used as a substitute.**

Prepared in accordance with ASME-14.100 — Selected item drawing

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| **REV** | | | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | | | | | | | | | | | | | | | | | | | | | | |
| **REV** | | | | | | | | | | | | | | | | | | | | | | |
| **PAGE** | | | | | | | | | | | | | | | | | | | | | | |
| **REV STATUS OF PAGES** | **REV** | | | | | | | | | | | | | | | | | | | | | |
| | **PAGES** | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | | | | | | | | | | |

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| **PMIC N/A** | **PREPARED BY**<br>Roger Kissel | **DEFENSE SUPPLY CENTER, COLUMBUS**<br>**COLUMBUS, OH**<br>**http://www.dscc.dla.mil/programs/milspec/docsearch.asp** |
| Original date of drawing<br><br>14 March 2005 | **CHECKED BY**<br>Alan Barone | **TITLE**<br>**SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, HIGH POWER TYPE 2N5927** |
| | **APPROVED BY**<br>Thomas Hess | |
| | **SIZE** A / **CODE IDENT. NO.** 037Z3 | **DWG NO.** 04029 |
| | **REV** | **PAGE** 1 **OF** 11 |

AMSC N/A

5961- E074

1. SCOPE

1.1 Scope. This drawing describes the requirements for NPN, silicon, high-power transistors.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

| 04029 | - | 01 | NONTX, TX, TXV |
|---|---|---|---|
| Drawing number | | Device type | Quality Level 1/ |

1.2.1 Device types. The device types identify the quality assurance level of the devices as follows:

| Device type | Figure number | Package |
|---|---|---|
| 04029-01 | 1 | Stud |
| 04029-01TX | 1 | Stud |
| 04029-01TXV | 1 | Stud |

1.3 Maximum rating. $T_C$ = +25°C unless otherwise specified.

| $P_T$ (1) $T_C$ = +25°C | $P_T$ (1) $T_C$ = +100°C | $V_{CEO}$ | $V_{CBO}$ | $V_{EBO}$ | $I_C$ (2) | $I_B$ | $T_J$ and $T_{STG}$ | $R_{\Theta JC}$ |
|---|---|---|---|---|---|---|---|---|
| W | W | V dc | V dc | V dc | A dc | A dc | °C | °C/W |
| 350 | 200 | 120 | 150 | 10 | 100 | 20 | -65 to +200 | 0.5 |

(1) Between $T_C$ = +25°C and $T_C$ = +200°C, linear derating factor (average) = 2.0 W/°C.
(2) Pulsed (see 4.4.1) = 120 A.

1.4 Primary electrical characteristics.

| $h_{FE}$ (1) | | | | $V_{BE}$ (1) | | $V_{CE(sat)}$ (1) | |
|---|---|---|---|---|---|---|---|
| $I_C$ = 120 A dc $V_{CE}$ = 4 V dc | $I_C$ = 70 A dc $V_{CE}$ = 2 V dc | $I_C$ = 40 A dc $V_{CE}$ = 2 V dc | $I_C$ = 20 A dc $V_{CE}$ = 2 V dc | $I_C$ = 70 A dc $V_{CE}$ = 2 V dc | $I_C$ = 120 A dc $V_{CE}$ = 4 V dc | $I_C$ = 70 A dc $I_B$ = 7 A dc | $I_C$ = 120 A dc $I_B$ = 24 A dc |
| Min 5.0 | Min 10 Max 40 | Min 15 Max 50 | Min 30 Max 120 | Max 1.5 | Max 3.0 | Max 0.75 | Max 2.0 |

(1) Pulsed (see 4.4.1).

| Limits | $R_{\Theta JC}$ | $\lvert h_{fe} \rvert$ $I_C$ = 5 A dc $V_{CE}$ = 10 V dc f = 100 KHz | $t_{on}$ | $t_s$ | $t_f$ |
|---|---|---|---|---|---|
| | °C/W | | $I_C$ = 70 A dc | | |
| Min | | 5 | | | |
| Max | .5 | 20 | 7.0 μs | 4.0 μs | 6.0 μs |

1/ Quality level: non-TX (-01 no suffix), -01TX, and -01TXV levels correspond to JAN, JANTX, and JANTXV equivalent quality requirements in MIL-PRF-19500.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-19500 and as specified herein.

3.1.1 Device capability. The devices must be capable of meeting the following MIL-STD-750 test conditions:

| Step | Method | Condition |
|---|---|---|
| 1 | 3053 | Load condition C (unclamped inductive load), $T_C$ = +25°C, single 10 ms pulse, $t_r$ = $t_f$ ≤ 1μs, $R_{BB1}$ = 1Ω, $R_{BB2}$ = ∞, $V_{BB1}$ = 6.2 V dc, $V_{BB2}$ = 0 V dc, $I_C$ = 50 A dc, $V_{CC}$ = 25 V dc, L = 5mH. See 3.1.2. Endpoints: Group A, subgroup 2. |
| 2 | 3053 | Load condition B (clamped switching destructive), $T_A$ = 25°C, single 2 ms pulse, $t_r$ = $t_f$ ≤ 1μs, $R_{BB1}$ = 1Ω, $R_{BB2}$ = 20Ω, $V_{BB1}$ = 8.5 V dc, $V_{BB2}$ = 3 V dc, $I_C$ = 70 A dc, $V_{CLAMP}$ = 125 V dc, L = 68 μH, $R_L$ = 0, clamping diode – 2N5926 with emitter shorted to base. Device fails if clamp voltage is not reached. See 3.1.2. Endpoints: Group A, subgroup 2. |
| 3 | 3051 | $T_C$ = 100°C, t = 1 s, 1 cycle, see 3.1.2 and figure 2.<br>Test 1 - $V_{CE}$ = 4 V dc, $I_C$ = 50 A dc<br>Test 2 - $V_{CE}$ = 50 V dc, $I_C$ = 4 A dc<br>Test 3 - $V_{CE}$ = 120 V dc, $I_C$ = 850 mA dc |
| 4 | 3131 | $I_M$ measurement ..... 10 mA.<br>$V_{CE}$ measurement voltage..... 25 V.<br>$I_H$ collector heating current..... 10 A.<br>$V_H$ collector-emitter heating voltage..... 20 V.<br>$t_H$ heating time ..... steady-state (see method 3131 of MIL-STD-750 for definition).<br>$t_{MD}$ measurement delay time..... 20μs maximum.<br>$t_{SW}$ sample window time..... 10μs maximum. |

3.1.2 Safe Operating Area (DC Operation) test. Each transistor shall sustain the applicable test conditions and the following acceptance criteria shall apply:

(a) $I_C$ (for each transistor) shall not vary more than ±10% during the dc operation; and

(b) All other specified end-point test(s) limits shall not be exceeded, after the dc-operation test.

(c) Correlation note: satisfactory endurance of the transistors throughout tests 1, 2, and 3 respectively (paragraph 3.1.1, step 3) is directly associable with ascertainment of the safe operating area for the transistors as illustrated in the nomograph of figure 2.

3.2 Abbreviations, symbol, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.3 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and figure 1 herein.

3.3.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein.

3.3.2 Internal construction. Multiple chip construction shall not be permitted.

3.4 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.5 Manufacturer eligibility. To be eligible to supply devices to this drawing, the manufacturer shall perform conformance inspection in accordance with the procuring activity's testing requirements as specified in 4.2 and 4.3 herein. Devices specified herein shall meet traceability as specified in MIL-PRF-19500. It is prohibited for a manufacturer not listed as an approved source to mark devices with this drawing number.

3.5.1 Certificate of compliance. A certificate of compliance shall be required from manufacturers requesting to be an approved source of supply.

3.5.2 Certificate of conformance. A certificate of conformance shall be provided with each lot of devices delivered in accordance with this drawing.

3.6 Recycled, recovered, or environmentally preferable materials. Recycled, recovered, or environmentally preferable materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.7 Workmanship. The semiconductor shall be uniform in quality and free from any defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Sampling and inspection. Unless otherwise specified, sampling and inspection procedures shall be performed in accordance with MIL-PRF-19500, and as specified herein.

4.2 Screening. All TX and TXV devices shall be screened in accordance with table IV of MIL-PRF-19500 as appropriate, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

| Screen (see table IV of MIL-PRF-19500) | Measurement |
|---|---|
| | TX and TXV levels |
| 4 | Optional |
| 9 | Not applicable |
| 11 | $I_{CES1}$ and $h_{fe1}$ |
| 12 | Burn-in (see 4.2.1). |
| 13 | $\Delta I_{CES1}$ = 100 percent of initial, maximum, subgroup 2 of table I herein;<br>$\Delta h_{FE1}$ = ±25 percent, maximum, subgroup 2 of table I herein. |

4.2.1 Power burn in. Power burn-in conditions are in accordance with method 1039 of MIL-STD-750, test condition B and as follows: $T_A$ = 30°C, ±5°C, $V_{CE} \geq$ 4.5 V dc, $T_J$ = 187.5°C ±12.5°C. NOTE: No heatsink or forced air cooling on the devices shall be permitted.

4.3 Conformance inspection. Conformance inspection shall consist of the inspections and tests specified in groups A and B herein.

4.3.1 Group A inspection. Group A inspection shall be conducted in accordance with the conditions specified for subgroup testing in table I herein.

4.3.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIb (JAN, JANTX and JANTXV) of MIL-PRF-19500 and table II herein. Electrical measurements (end-points) and delta requirements shall be table I, subgroup 2 herein or as specified.

4.3.2.1 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B for non-TX, TX, and TXV) may be pulled prior to the application of final lead finish.

4.4 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.4.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

| Inspection 1/ | MIL-STD-750 | | Symbol | Limit | | Unit |
|---|---|---|---|---|---|---|
| | Method | Conditions | | Min | Max | |
| Subgroup 1 | | | | | | |
| Visual and mechanical inspection | 2071 | | | | | |
| Subgroup 2 | | | | | | |
| Breakdown voltage, collector to emitter | 3011 | Bias condition D; $I_C$ = 200 mA dc; pulsed (see 4.4.1) | $V_{(BR)CEO}$ | 120 | | V dc |
| Collector to base cutoff current | 3041 | Bias condition C; $V_{BE}$ 0 V dc; $V_{CE}$ = 150 V dc | $I_{CES1}$ | | 2 | mA dc |
| Emitter to base current | 3061 | Bias condition D; $V_{EB}$ = 10 V dc | $I_{EBO}$ | | 1 | mA dc |
| Base emitter voltage | 3066 | Test condition B, $I_C$ = 70 A dc, $V_{CE}$ = 2 V dc, pulsed (see 4.4.1) | $V_{BE1}$ | | 1.5 | V dc |
| Base emitter voltage | 3066 | Test condition B, $I_C$ = 120 A dc, $V_{CE}$ = 4 V dc, pulsed (see 4.4.1) | $V_{BE2}$ | | 3.0 | V dc |
| Saturation voltage and resistance | 3071 | $I_C$ = 70 A dc; $I_B$ = 7 A dc; pulsed (see 4.4.1) | $V_{CE(SAT)1}$ | | 0.75 | V dc |
| Saturation voltage and resistance | 3071 | $I_C$ = 120 A dc; $I_B$ = 24 A dc; pulsed (see 4.4.1) | $V_{CE(SAT)2}$ | | 2.0 | V dc |
| Forward-current transfer ratio | 3076 | $V_{CE}$ = 2 V dc; $I_C$ = 20 A dc pulsed (see 4.4.1) | $h_{FE1}$ | 30 | 120 | |
| Forward-current transfer ratio | 3076 | $V_{CE}$ = 2 V dc; $I_C$ = 70 A dc pulsed (see 4.4.1) | $h_{FE2}$ | 10 | 40 | |
| Forward-current transfer ratio | 3076 | $V_{CE}$ = 2 V dc; $I_C$ = 40 A dc pulsed (see 4.4.1) | $h_{FE3}$ | 15 | 50 | |
| Subgroup 3 | | | | | | |
| High-temperature operation | | $T_A$ = +150°C; n = 15, c = 0 | | | | |
| Collector-base cutoff current | 3041 | Bias condition C; $V_{CE}$ = 100 V dc, $V_{BE}$ = 0 V dc | $I_{CES2}$ | | 10 | mA dc |
| Low-temperature operation | | $T_A$ = -65°C | | | | |
| Forward-current transfer ratio | 3076 | $V_{CE}$ = 2 V dc; $I_C$ = 70 A dc; pulsed (see 4.4.1) | $h_{FE4}$ | 10 | | |

See footnote at end of table.

TABLE I. Group A inspection - Continued.

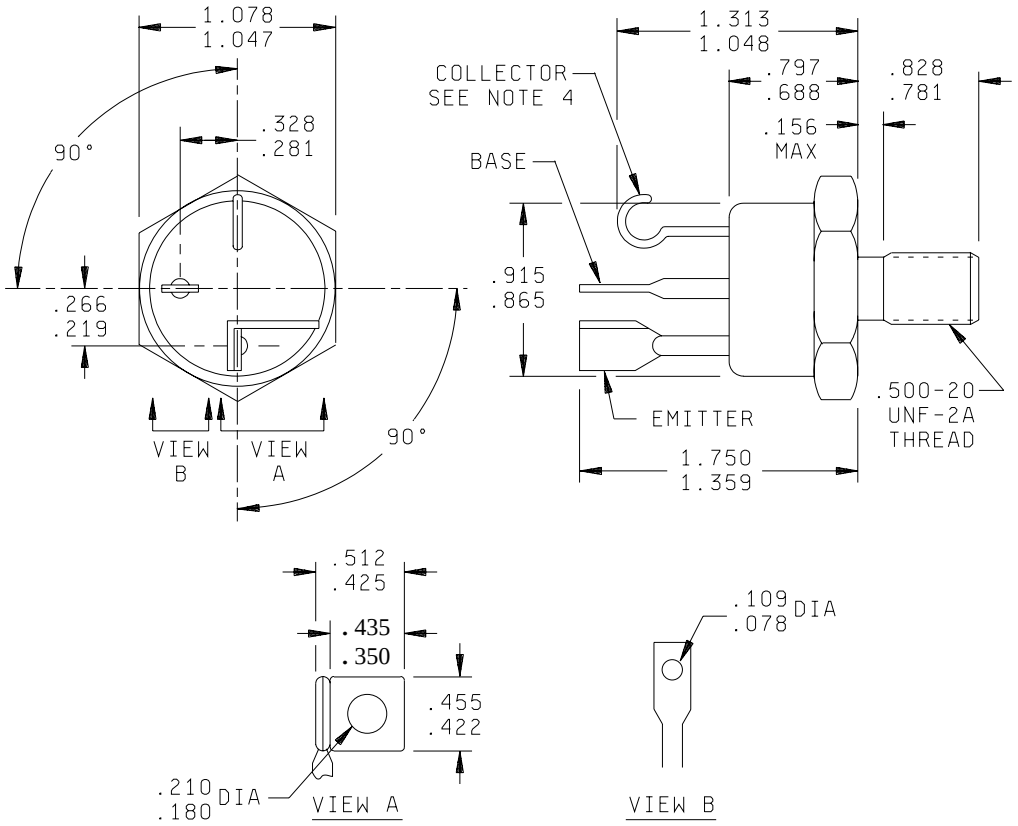
| Inspection 1/ | MIL-STD-750 | | Symbol | Limit | | Unit |
|---|---|---|---|---|---|---|
| | Method | Conditions | | Min | Max | |
| Subgroup 4 | | | | | | |
| Pulse response | 3251 | Test condition B, $V_{CC}$ = 70 V dc, $R_c$ = 1 Ω, $V_{BE1}$ = 8.5 V dc, $R_b$ = 1 Ω, $V_{BE2}$ = 10 V dc; n = 15, c = 0 | | | | |
| Turn-on time | | | $t_{on}$ | | 7.0 | µs |
| Turn-off time | | | $t_s$ | | 4.0 | µs |
| Fall time | | | $t_f$ | | 6.0 | µs |
| Magnitude of common emitter small signal short-circuit forward-current transfer ratio | 3306 | $V_{CE}$ = 10 V dc; $I_C$ = 5 A dc; f = 100 kHz | $\|h_{fe}\|$ | 5 | 20 | |
| Subgroups 5, 6 and 7 | | | | | | |
| Not applicable | | | | | | |

1/ See MIL-PRF-19500 for sampling plan.

TABLE II. Group B inspection for TX and TXV.

| Inspection 1/ | MIL-STD-750 | | Small lot CI |
|---|---|---|---|
| | Method | Conditions | |
| Subgroup 1 | | | |
| Solderability | 2026 | | |
| Resistance to solvents | 1022 | | n = 3, c = 0 |
| Subgroup 2 | | | |
| Temperature cycling (air to air) | 1051 | Test condition C | n = 6, c = 0 |
| Hermetic seal | 1071 | | |
| Fine leak<br>Gross leak | | | |
| Electrical measurements | | See table I, subgroup 2 herein. | |
| Subgroup 3 | | | |
| Steady state operation life | 1027 | $T_A$ = 30°C ± 5°C, $V_{CE} \geq$ 4.5 V dc, $T_J$ = 187.5°C, ±12.5°C, 168 hours minimum | n = 12, c = 0 |
| Electrical measurements | 3041<br>3076 | $\Delta I_{CES1}$ = +100% of initial value, maximum<br>$\Delta h_{FE1}$ ±25 percent change of initial value, maximum | |
| Subgroup 4 | | | |
| Decap internal visual (design verification) | 2075 | | n = 1, c = 0 |
| Subgroup 5 | | | |
| Thermal resistance | 3131 | $R_{\Theta JC}$ = .5°C/W; see 3.1.1 | n = 6, c = 0 |
| Subgroup 6 | | | |
| High-temperature life (nonoperating) | 1032 | t = 168 hours minimum, T = +200°C | n = 12, c = 0 |
| Electrical measurements | | See table I, subgroup 2 herein | |

1/ For sampling plan, see MIL-PRF-19500.




NOTES:
1. Dimensions are in inches.
2. Maximum pitch diameter of plated thread shall be basic pitch diameter (.4675 inch).
3. Angular orientation of terminals with respect to hex flats is optional.
4. Collector shall be electrically connected to the case.

FIGURE 1. Physical dimensions.

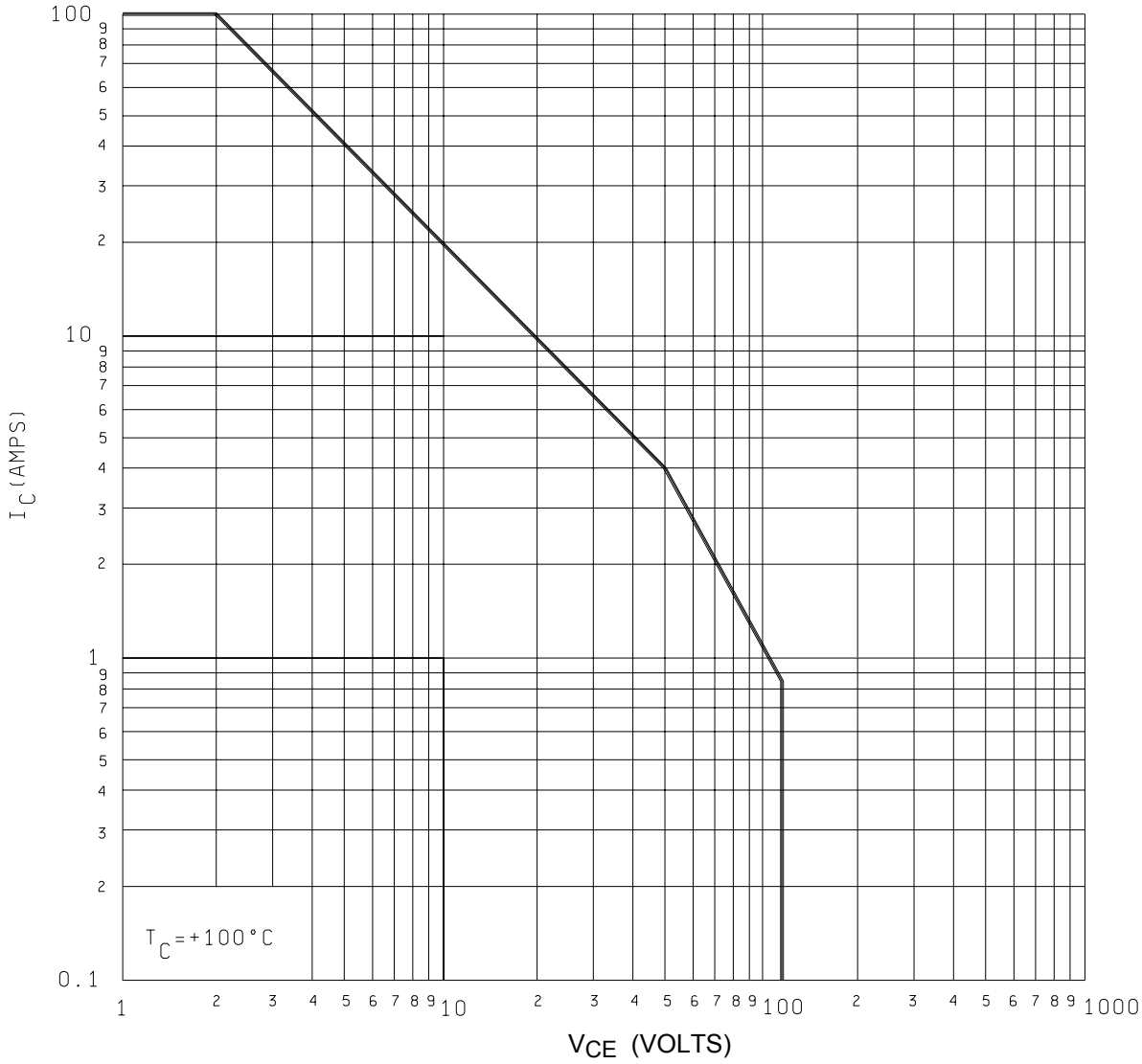



FIGURE 2. Maximum safe operating graph (continuous dc).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

6.1 Intended use. Devices conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. This drawing is intended exclusively to prevent the proliferation of unnecessary duplicate specifications, drawings, and stock catalog listings. When a product covered by this drawing has been listed on QML-19500, this drawing will be inactivated and will not be used for new design. The QML-19500 products shall be the preferred item for all applications.

6.2 Acquisition requirements. The acquisition requirements should specify the following:

a. Complete PIN (see 1.2).

b. Requirements for delivery of one copy of the conformance inspection data or certificate of compliance that parts have passed conformance inspection with each shipment of parts by the manufacturer.

c. Requirements for packaging and packing.

6.3 Replaceability. Devices covered by this drawing replace the same device covered by specification sheet MIL-S-19500/440, which has been cancelled.

6.4 Comments. Comments on this drawing should be directed to Defense Supply Center Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, e-mail Semiconductor@dscc.dla.mil or telephone (614) 692-0510.

6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have passed the requirements of section 4 herein and have submitted a certificate of compliance to DSCC-VAC.

| DSCC drawing PIN (1) | JEDEC numbers | Vendor CAGE code | Vendor name and address |
|---|---|---|---|
| 04029-01<br>04029-01TX<br>04029-01TXV | 2N5927<br>2N5927<br>2N5927 | 32953 | Power Tech Incorporated<br>0-02 Fair Lawn Avenue<br>Fair Lawn NJ 07410-1281 |

(1) Parts must be purchased to this DSCC PIN to assure that all performance requirements and tests are met.